WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a plurality of first signal lines formed on the insulating substrate;

a plurality of second signal lines formed on the insulating substrate, insulated from the first signal lines, and intersecting the first signal lines;

a plurality of third signal lines formed on the insulating substrate, insulated from the second signal lines, and intersecting the second signal lines;

a plurality of pixel electrodes provided on respective pixel areas defined by the intersections of the first and the second signal lines, each pixel electrode having a cutout;

a plurality of direction control electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines;

a plurality of first thin film transistors, each first thin film transistor connected to one of the first signal lines, one of the second signal lines, and one of the pixel electrodes; and

a plurality of second thin film transistors, each second thin film transistor connected to one of the first signal lines, one of the third signal lines, and one of the direction control electrodes.

2. The thin film transistor array panel of claim 1, wherein one of the first thin film transistors and one of the second thin film transistor located on one of the pixel areas are connected to a relevant one of the first signal lines and a previous one of the first signal lines.

3. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including first and second gate electrodes and a plurality of gate lines;

a storage electrode wire formed on the insulating substrate and including a plurality of storage electrode lines and a plurality of storage electrodes;

a gate insulating layer formed on the gate wire and the storage electrode wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a plurality of data lines intersecting the gate lines, a plurality of first source electrodes connected to the data lines, a plurality of first drain electrodes opposite the first source electrodes with respect to the first gate electrodes, a plurality of second source electrodes electrically connected to the storage electrode wire, and a plurality of second drain electrodes opposite the second source electrodes with respect to the second gate electrodes;

a direction control electrode connected to the second drain electrode;

a passivation layer formed on the data wire and the direction control electrode and having a plurality of contact holes; and

a pixel electrode formed on the passivation layer, having a plurality of cutouts, and electrically connected to the first drain electrodes through the contact holes.

4. The thin film transistor array panel of claim 3, where in the direction control electrode overlaps the cutouts of the pixel electrode at least in part.

5. The thin film transistor array panel of claim 4, wherein the cutouts of the pixel electrode comprise a plurality of X-shaped cutouts and a plurality of rectilinear cutouts and the direction control electrode overlaps the X-shaped cutouts.

6. The thin film transistor array panel of claim 4, wherein the semiconductor layer comprises a plurality of data portions disposed under the data lines, a plurality of first channel portions disposed under the first source electrodes and the first drain electrodes, and a plurality of second channel portions disposed under the second source electrodes and the second drain electrodes.

7. The thin film transistor array panel of claim 3, further comprising a plurality of connecting members formed on the passivation layer

and connecting the second source electrodes and the storage electrode wire through contact holes provided at the passivation layer and the gate insulating layer.

8. The thin film transistor array panel of claim 4, wherein the direction control electrode includes substantially the same layer and material as the data wire.

9. A liquid crystal display comprising:

a first insulating substrate;

a plurality of first signal lines formed on the first insulating substrate;

a plurality of second signal lines formed on the first insulating substrate, insulated from the first signal lines, and intersecting the first signal lines;

a plurality of third signal lines formed on the first insulating substrate, insulated from the second signal lines, and intersecting the second signal lines;

a plurality of pixel electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines, each pixel electrode having a cutout;

a plurality of direction control electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines;

a plurality of switching elements, each first switching element connected to one of the first signal lines, one of the second signal lines, and one of the pixel electrodes;

a plurality of second thin film transistors, each second switching element connected to one of the first signal lines, one of the third signal lines, and one of the direction control electrodes;

a second insulating substrate opposite the first insulting substrate;

a common electrode formed on the second insulating substrate; and

a liquid crystal layer interposed between the first insulating substrate and the second insulating substrate.

10. The liquid crystal display of claim 9, wherein the third signal lines are supplied with a voltage to be applied to the common electrode.

11. The liquid crystal display of claim 10, wherein the liquid crystal layer has negative dielectric anisotropy and major axes of liquid crystal molecules in the liquid crystal layer are aligned vertical to the first and the second substrates.

12. The liquid crystal display of claim 10, wherein the liquid crystal layer has positive dielectric anisotropy and major axes of liquid crystal molecules in the liquid crystal layer are aligned parallel to the first and the second substrates.

13. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate;

a storage electrode wire formed on the insulating substrate;

a gate insulating layer formed on the gate wire and the storage electrode wire;

a data wire formed on the gate insulating layer including three layers an amorphous silicon layer, a doped amorphous silicon layer, and a metal layer;

a direction control electrode formed on the gate insulating layer, including three layers an amorphous silicon layer, a doped amorphous silicon layer, and a metal layer, and electrically connected to the second drain electrode;

a passivation layer formed on the data wire and the direction control electrode and having a plurality of contact holes; and

a pixel electrode formed on the passivation layer, having a plurality of cutouts, and electrically connected to the data wire through the contact holes.

14. The thin film transistor array panel of claim 13, wherein the gate wire comprises first and second gate electrodes, the data wire comprises first and second source electrodes and first and second drain electrodes, the direction control electrode is connected to the second drain electrode, the pixel electrode is connected to the first drain electrode, and the second source electrode is connected to the storage electrode wire.

15. The thin film transistor array panel of claim 14, further comprising a connecting member formed on the passivation layer and connecting

the second source electrode and the storage electrode wire through a contact hole provided at the passivation layer and the gate insulating layer.

16. A method of manufacturing a thin film transistor array panel, comprising:

forming a gate wire and a storage electrode wire;

depositing a gate insulating layer, an amorphous silicon layer, a contact layer, and a metal layer;

patterning the metal layer, the contact layer, and the metal layer to form a data wire, a direction control electrode, and a channel portion of a thin film transistor;

forming a passivation layer on the channel portion; and

forming a pixel electrode and a connecting portion on the passivation layer.